Vidhyayana - ISSN 2454-8596
An International Multidisciplinary Peer-Reviewed E-Journal
www.vidhyayanaejournal.org
Indexed in: Crossref, ROAD & Google Scholar

14

# Resistance Measurement Using Sample and Hold Method

**Kajal Chavda**

Research Scholar, Department of Physics, Surendranagar University, Gujarat

**Dr. Achal Kiran**

Assistant Professor, Department of Physics, Surendranagar University, Gujarat

**Abstract:**

In electronics, a sample and hold circuit is an analog device that samples (captures, takes) the voltage of a continuously varying analog signal and holds (locks, freezes) its valve at aconstant level for aspecified minimum period of time.This circuits are typically Used in analog-to-digital converters to eliminate variations in input signal that can corrupt the conversion process.

**Resistance Measurement Using Sample and Hold Method**

A sample and hold circuit, as the name implies, sample an analogue input is signal and holds its value until the input is again sampled. Here we use sample and method for resistance measurement.

A Sample or hold circuit.

Vidhyayana - ISSN 2454-8596
An International Multidisciplinary Peer-Reviewed E-Journal
www.vidhyayanaejournal.org
Indexed in: Crossref, ROAD & Google Scholar

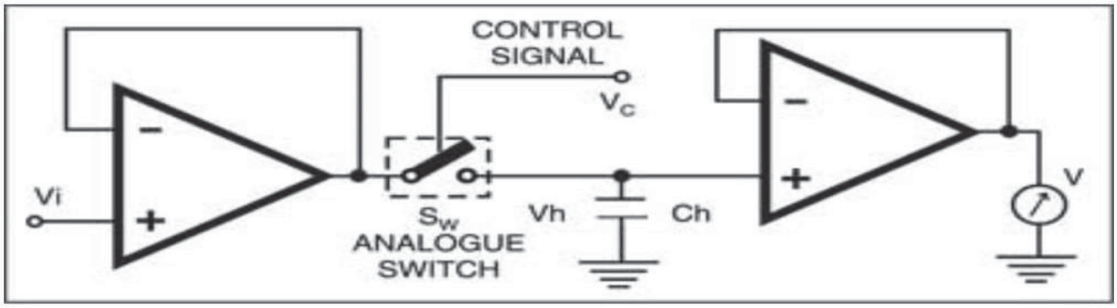


*Fig. 1: A typical sample and hold circuit*

Fig-1 shows the basic principal of the sample and hold circuit. The analogue signal Vi applied to non-inverting unity-gain amplifier built around an op-amp. This amplifier acts as a buffer. The control terminal of analogue switch Sw decides whether the switch will be closed or open.

When the control terminal is held at logic 1, the switch is closed(on). The time for which the switch remainsON is called the sampling period (Ts). During the sampling period, the hold capacitor (Ch) changes up very quickly through the low on resistance of the analogue switch (typically, a few hundred ohms) and follow the analogue voltage at every instant (refer fig-2).

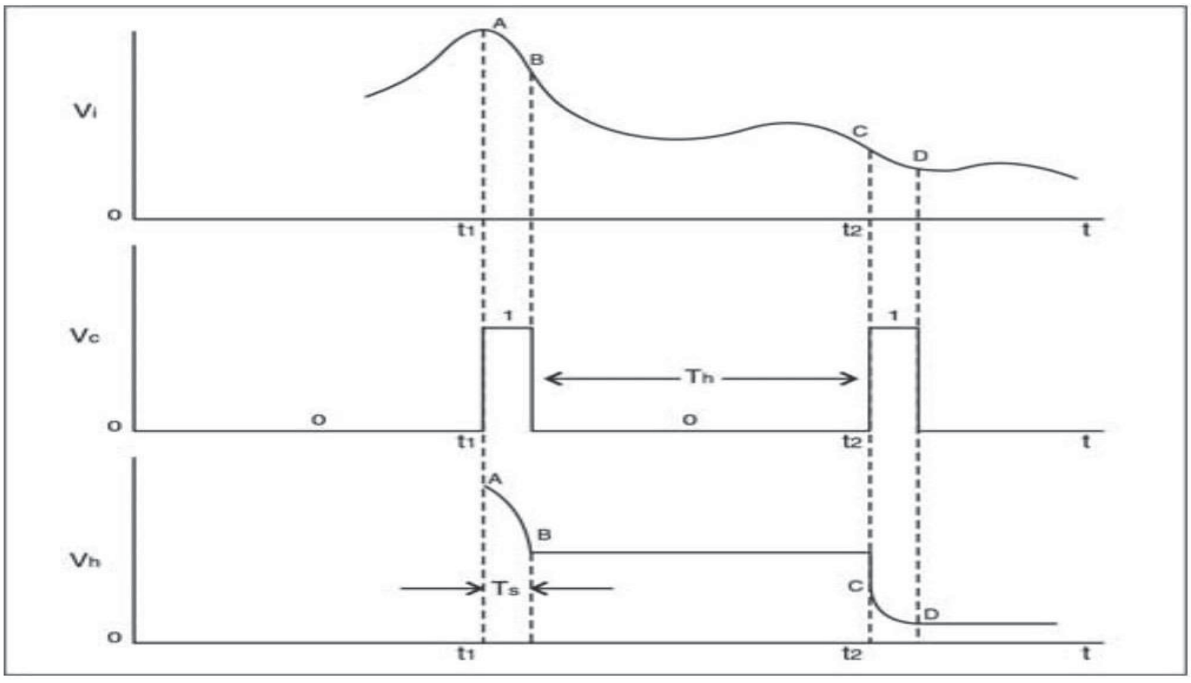


*Fig. 2: Waveforms of input signal, control signal, and sample and hold signal*

Vidhyayana - ISSN 2454-8596
An International Multidisciplinary Peer-Reviewed E-Journal
www.vidhyayanaejournal.org
Indexed in: Crossref, ROAD & Google Scholar

When the control terminal is held at logic 0, the switch becomes open(off)and the sampling period ends. The period for which the switch remains off is called the hold period (Th). The voltage across hold capacitor Ch is fed to a buffer built around another op-amp.

During period Th, hold capacitor Ch hold the latest value of the analogue voltage(the value just before the switch is turned off) because it does not find any path to discharge.On the left side it find the exceedingly large resistance of the off CMOS switch (several hundreds ofmega-ohms). And on the right side it finds the high input resistance of the buffer (about 105 mega-ohms).So the only path to discharge is its own natural leakage resistance. Using a Mylar or Teflon capacitor,we can realize a very high leakage resistance in mega-ohms. Thus the voltmeter holds the most recent value of the sampled analogue voltage until we go for the next sampling.

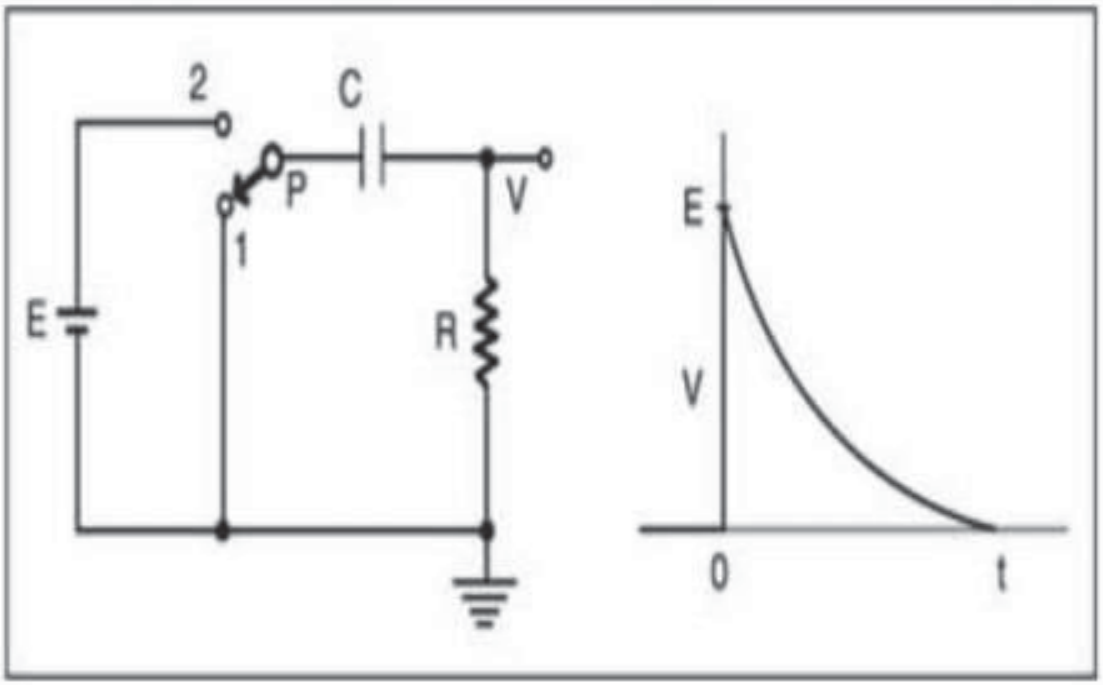


*Fig. 3: Capacitor charging circuit and its exponential curve*

Vidhyayana - ISSN 2454-8596
An International Multidisciplinary Peer-Reviewed E-Journal
www.vidhyayanaejournal.org
Indexed in: Crossref, ROAD & Google Scholar

**Resistance measurement using sample or hold circuit:**

The sample and hold circuit can be used for resistance measurement by charging a capacitor (refer fig3). Initially, the timing capacitor C is uncharged. As the pole(p) of the DPDT switch leaves contact 1 and touches contact2, the output voltage(v) immediately attains the battery voltage (E) (Recall that the voltage across acapacitor cannot be changed instantaneously) The capacitor now begins to charge up and the voltage v begins to decrease exponentially, viz,

$V=Ee^{-t/tau}$

Where t is the time constant of the R-C circuit, i.e., Tau=RC.

Fig 4 shows the necessary circuit. Here we have used national semiconductors ICLF398(IC2) for the sample and hold circuit. IC NE555(IC1) is used as an astable multivibrator generating a square wave. Its on time is given by:

$T_{on}=R_A C_T \ln 2$

Where ln stands for natural log.

This is previously introduced sampling time (Ts) and is about 0.5 second.

The off time of the multivibrator is:

$T_{off}=VR_B C_T \ln 2$

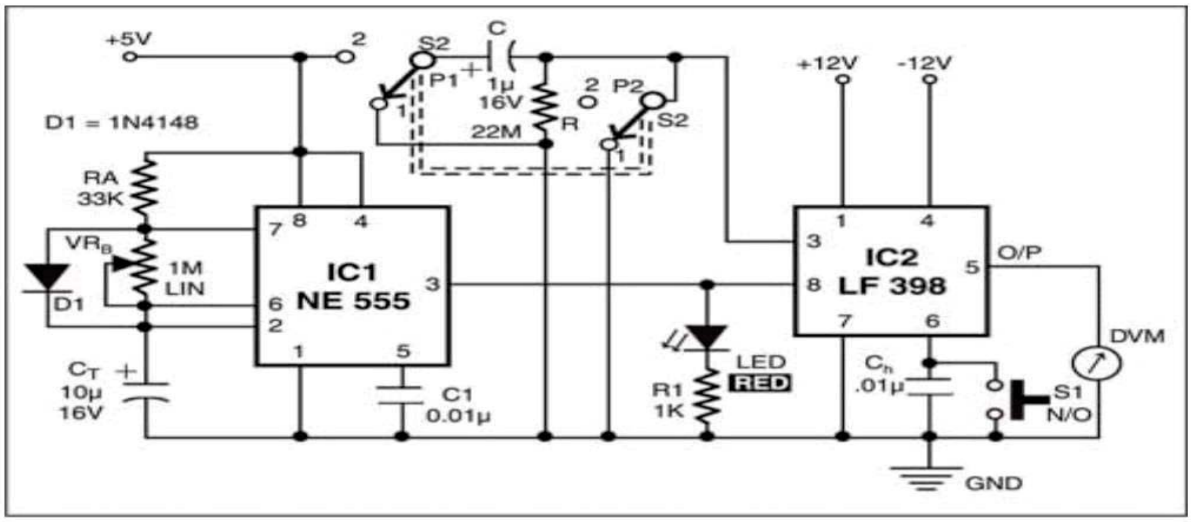


*Fig. 4: The sample and hold circuit for resistance measurement*

Vidhyayana - ISSN 2454-8596
An International Multidisciplinary Peer-Reviewed E-Journal
www.vidhyayanaejournal.org
Indexed in: Crossref, ROAD & Google Scholar

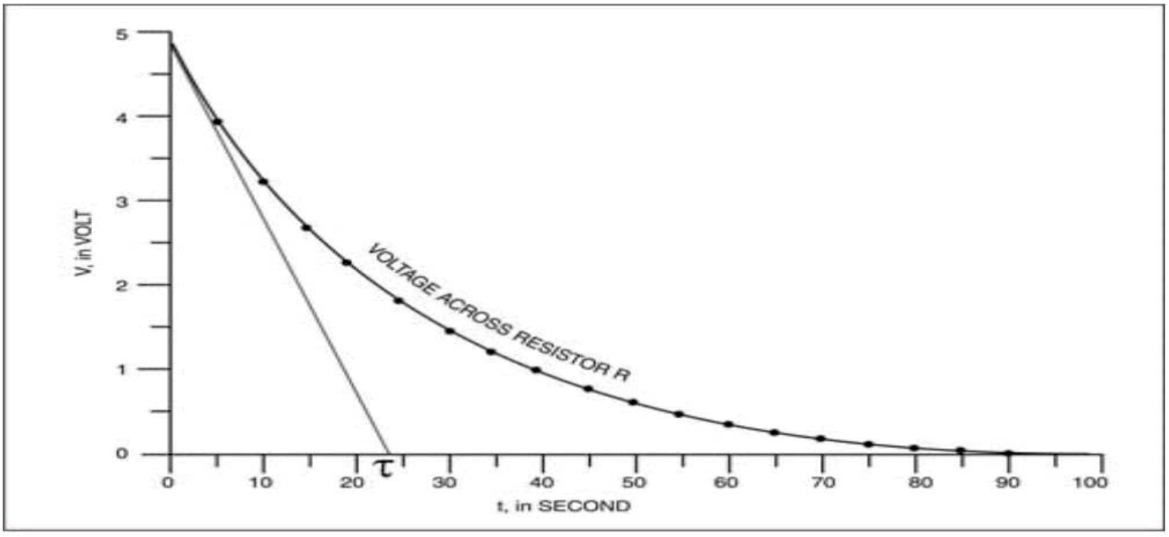


*Fig. 5: The voltage measured at different times*

This is the hold period (Th). Using a 1 mega ohm linear potentiometer, $VR_B$is adjusted to make Th close to 5 seconds.

First, momentarily press normally-open(N/O) switch S1 so as to discharge hold capacitor Ch and then release it. Keep DPDT switch S2in Down position, so both the poles are in touch with their respective contact 1`. This makes the capacitor C fully discharged and it is ready for placement in the charging circuit.

Carefully observe the blinking of the LED for at least three cycles. Its flashing rate will give you an idea of the sample and hold period when the LED flashes up for a split second, toggle the DPDT switch to up position, so both the poles will touch their respective contact2.

You can now notice the accurate status of the capacitor. The voltage across resistor R is the analogue voltage you want to measure this voltage regularly at an interval of 5 second until the capacitor is fully charged and the voltage across the resistor drops to zero with C=1f and R=22 mega-ohms, it takes about four time constants, which is about 90 second for the capacitor to fully charge up.

Vidhyayana - ISSN 2454-8596
An International Multidisciplinary Peer-Reviewed E-Journal
www.vidhyayanaejournal.org
Indexed in: Crossref, ROAD & Google Scholar

TABLE

| S. No. | Time t, in seconds | Voltage across it in Volt |
|---|---|---|
| 1 | 0 | 4.95 |
| 2 | 5 | 3.88 |
| 3 | 10 | 3.06 |
| 4 | 15 | 2.41 |
| 5 | 20 | 1.89 |
| 6 | 25 | 1.49 |
| 7 | 30 | 1.16 |
| 8 | 35 | 0.90 |
| 9 | 40 | 0.69 |
| 10 | 45 | 0.53 |
| 11 | 50 | 0.40 |
| 12 | 55 | 0.30 |
| 13 | 60 | 0.22 |
| 14 | 65 | 0.15 |
| 15 | 70 | 0.10 |
| 16 | 75 | 0.06 |
| 17 | 80 | 0.03 |
| 18 | 85 | 0.01 |
| 19 | 90 | 0.00 |

Draw the measured voltage values (across)against their respective times (refer fig 5and table). The tangent drawn to the curve at the origin (t=0)intersects the tie axis at t=22second,i.e=22 second,since c is 1 Micro f,the measured value of resistor Ris close to 22 mega ohms. This is an excellent agreement.

The natural leakage resistance of the Mylar capacitor C is very large and does not contribute in the measurement.

This circuit costs around Rs. 135.

**REFERENCES:**

1. Sodha, M.S., Dang, A., Bansal, P.K., and Sharma, S.B., An analytical and experimental study of open sun drying and a cabinet type dryer, energy conversion and management,25,263(1985).
2. Sodha, M.S., Kumar A., Tiwari G.N., and Tyagi, R.C., simple multi-wick solar still: Analysis and Performance, Solar energy,26,127, (1981b).
3. Tiwari, G.N. and Goyal R.K., Greenhouse Technology, Narosa publishing House, New Delhi (1998).
4. Tiwari, G.N. and Sangeeta Suneja, Solar Thermal Engineering System, Narosa Publishing House, New Delhi (1997).
5. Toyama, S., Agraki, T., Slish, H.M., Murase, K., and Sando, M., Simulation of Multi-effect Solar still and the Static characterеistics, J. of chem. Engg., Japan, 20, 473(1987).
6. Toyama, S., Kagaku Kikai, Gijtsu,24, 159, Mauzen, Tokyo (1972).
7. United Nations, Solar Distillation, Department of Economies or Social Affair, New York (1976).
8. Zandi, Z.M., Portable Titled Solar Still, Sun World, 6(1),6(1982).